Towards Structural Testing of Superconductor Electronics

Arun A. Joseph and Hans G. Kerkhoff

Testable Design and Testing of Microsystems Group, MESA+ Research Institute,
University of Twente, 7500 AE Enschede, The Netherlands.
E-mail: {A.A.Joseph, H.G.Kerkhoff}@el.utwente.nl

Abstract

Many of the semiconductor technologies are already facing limitations while new-generation data and telecommunication systems are implemented. Although in its infancy, superconductor electronics (SCE) is capable of handling some of these high-end tasks. We have started a defect-oriented test methodology for SCE, so that reliable systems can be implemented in this technology. In this paper, the details of the study on the Rapid Single-Flux Quantum (RSFQ) process are presented. We present common defects in the SCE processes and corresponding test methodologies to detect them. The (measurement) results prove that we are able to detect possible random defects for statistical purposes in yield analysis. This paper also presents possible test methodologies for RSFQ circuits based on defect oriented testing (DOT).

1. Introduction

Requirements for efficient new-generation electronic systems in data and telecommunication industries are pushing the semiconductor technologies to their limits. In the near future, current semiconductor technologies will not always be able to provide efficient solutions for the speed, accuracy and power requirements. Applications such as Software-Defined Radio (SDR) [1], petaflop computers [2] and high-speed network routers [3] are extremely difficult to implement and are very complex in nature. Even at this immature stage, superconductor electronics (SCE) is capable of handling these tasks. Having a very high theoretical speed limit (~1 THz) with the accuracy of a magnetic flux quantum (2.07 x 10e-15 Wb) and very-low power consumption (~1 pW/gate), SCE is a promising candidate for the above-mentioned applications. Disadvantage of an SCE system is the requirement of cooling the device to super-conducting temperatures. But the above-mentioned applications require cooling even if semiconductor technologies are used and intense research is carried out to bring the SCE systems like an Analog-to-Digital converter (ADC) to "high" temperatures by developing them in high-temperature superconductor (HTS) technology [4].

A number of commercial enterprises have started developing systems in SCE. IBM was one of the first to start research in SCE. But the project was abandoned due to pre-mature technology for realizing these SCE circuits. Later, after the invention of Rapid Single-Flux Quantum (RSFQ) logic [5], and the development of the planar tri-layer process [6], the limitations in realizing LSI SCE circuits were eliminated. In the past few years, extensive research has been carried out with regard to the development of high-end complex systems in SCE. Examples of these complex designs are a superconductor ADC [7] targeted towards SDR developed by HYPRES Inc. NY, the Flux microprocessor chip [8] for the US defense petaflops program by TRW Space and Electronics (now Northrop Grumman, CA) and a GHz packet switch [9] by NEC, Japan for high-speed networks.

As the complexity of the circuits is increasing, the realization of the design becomes a difficult task. Although extended research is going on in making complex circuits and scaling down the minimum sizes, very little or no information is available in the literature on the methodology for defect analysis for superconductor electronics. The yield levels are currently much lower than in the semiconductor industry. This is due to the fact that while much research has been carried out with respect to the defects in semiconductor manufacturing processes [10], little information is available on superconductor processes.

In semiconductor microelectronics, special test structures have been developed and realized along with the functional integrated circuits. The information gathered using these test structures are used for yield analysis and defect-oriented testing [11]. Fault models have been developed after studying the behaviour of the test structures. These fault models are subsequently used for ATPG and fault simulation of the circuit. In this way, the

semiconductor industry has developed methodologies and techniques to achieve high yields.

Our ultimate goal is to develop ATPG for SCE logic circuits. Investigating the possibility of whether or not the available ATPG techniques are applicable is one of the major concerns in the process. Otherwise new ATPG techniques have to be developed for SCE. Information about defects and their subsequent translation into fault-models are crucial at this stage. At this moment, little is known about the defects that can occur in an SCE fabrication process.

We have developed a test methodology for defect analysis in SCE. Major issues handled during the development process were test-ease and test-time, which are measures of test cost. For this purpose, we studied two RSFQ processes and subsequent results are presented. In this paper, we present the test results on structures that have been developed to detect the top-ranking defects that can occur in a Niobium tri-layer based technology. Based on this information, we have also conducted DOT and those results are presented leading to possible test methodologies for RSFQ circuits.

The organization of the paper is as follows. The next section briefly explains defects and the required testing strategies. In section 3, RSFQ circuits and the processes that were under study are described, followed by the defect detection in section 4. Associated Defect-Oriented testing (DOT) techniques for RSFQ circuits that have been carried out are described in section 5. Experimental results and conclusions are presented in the final sections.

2. Defects and Structural Testing

Design errors and manufacturing defects are the two types of defects that can occur in an IC manufacturing process flow. For process-defect analysis, manufacturing defects are considered. It can be further classified as local (random) defects and gross manufacturing defects. Defects that affect a large area, even a complete wafer, are called gross manufacturing errors, which is characteristic for an immature process. Detection of local defects, occurring random in nature, is important because they contribute to the majority of the defects in a matured manufacturing process.

The most common structural defects that occur in a silicon-based IC manufacturing process are:

1. Shorts between metal layers
2. Opens in metal layers

Intralayer shorts (between the same metal layer) occur resulting from extra material and formation of interlayer shorts (between different metal layers) is due to bad isolation layers. Opens in layers or in vias result from the absence of material; cracking of metal layers due to step-coverage problems is another issue, which, in the worst case, can become an open in the layer.

The effective detection and avoidance of these defects in a manufacturing process is essential for the quality of the devices developed in that technology. Information about these defects in a process is gathered by using specially designed test modules also called Process Defect Monitors (PDM), which consist of a number of test structures. There are four types of test structures: the first type is for evaluating the functional properties of IC building blocks (test circuits). The other types are for the extraction of IC geometric parameters like dimensions, the determination of the structural defect distribution and their influence on yield (short, breaks etc.) and for the determination of electrical parameters like e.g. the threshold voltage (Vth).

In this paper, we will discuss the third type of test structures. The information gathered using this structure is the basis for DOT. Inductive fault analysis (IFA) is a widely used technique for DOT.

3. RSFQ Circuits and Defects in Processing

Essential elements in an RSFQ circuit are Josephson Junctions (JJ), inductors and resistors for biasing and shunting the junction. A JJ, the basic active element of an SCE circuit, is formed when two superconductors are separated by an interface of nanometer dimensions. Operation of a JJ is based on the quantum mechanical tunneling across this dielectric barrier [12]. Inductors are of two types, storage and normal (non-storage). Storage inductances have relatively higher values, so that the loop containing a JJ will be able to store a magnetic flux quantum or a fluxon. RSFQ circuits use very little power because they remain in super-conducting state except while switching during operation, which lasts only for a few pico-seconds. A negative bias voltage, resulting in a negative bias current, is applied to the RSFQ circuit for the correct operation.

In RSFQ digital logic, information is interpreted as follows. All signals are in the form of a pulse, called an SFQ pulse. A clock signal (also an SFQ pulse) is the signal that determines the state of the circuit. In other words, the state of a circuit is determined by looking at the clock signals along with the I/O SFQ pulses. The input state of the circuit is said to be "HIGH" if an input signal arrives between two clock pulses at that particular instance and otherwise "LOW". Similarly the output is "HIGH" if a signal is emitted between two clock pulses and "LOW" otherwise. Detailed information on RSFQ logic is given in reference [5].

Design and layout procedures in SCE are similar to that in semiconductor electronics, in fact they are much less complex compared to the latest 10+ interconnect-layer processes in semiconductor industry. For the design and implementation of RSFQ circuits, a number of tools have been developed in the past. A set of tools has been recently integrated into the CADENCE design environment [13]. With these advanced CAD facilities, a direct systematic implementation of complex systems can be carried out with ease.

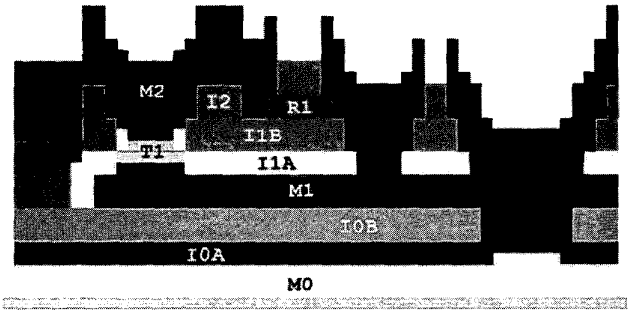

Fig. 1. Cross-section of the FOUNDRY1 process.

The first RSFQ process that we have been investigating is an academic tri-layer process, hereby denoted as FOUNDRY1 process. It has got three Niobium (Nb) metal layers including the ground plane (M0, M1 and M2). A cross-section of the process is shown in Fig.1. The minimum dimensions for interconnection width and spacing are 5 μm. The critical current density Jc for the process is 1 kA/cm^2 and the sheet resistance of the Molybdenum resistor layer is 1 Ω/square. The junction capacitance for the process is 0.05 pF/μm^2.

The second process under study is that from a commercial company, denoted as FOUNDRY2 process. This is a more matured commercial process, but quite similar to that of FOUNDRY1 process. It has got 4 Nb metal layers M0, M1, M2 and M3, M0 being the ground plane. There are two standard Jc values for this process being 1 kA/ cm^2 and 5 kA/ cm^2 and the minimum feature-size is 2.5 μm. The junction capacitances are 0.06 pF/μm^2 and 0.05 pF/μm^2 for 1 and 5 kA/cm^2 respectively. Additional advantage is that M3 can be used as a second ground plane to design more stable circuits. The cross-section of the process is given in Fig. 2.

Table I shows the layers in both processes. The layer name corresponds to that in Fig. 1 and Fig. 2. The Nb metal layer is deposited over the silicon substrate as ground plane. After the isolation layers and M1, the tri-layer is created using a single mask. It actually consists of a sandwich of 3 layers, two Nb layers acting as the electrodes with the Al_2O_3 sandwich in-between. This is carried out so as to minimize the formation of pinholes in the thin barrier. In both the processes a double isolation is carried out so as to reduce the pinhole formation in the isolation leading to interlayer shorts.

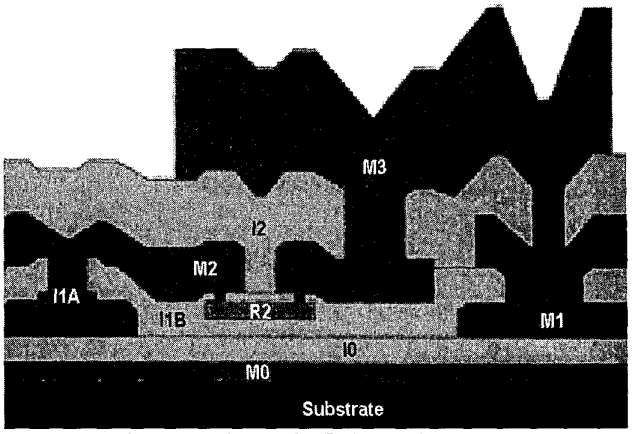

Fig. 2. Cross-section of the FOUNDRY2 process.

Until now, most research has been carried out on parametric defects in superconductor processes and the functional verification of devices. As the processes become more mature, the importance of detecting the structural defects increases. This is due to the fact that the occurrence of gross manufacturing errors and deviation of parametric values are decreasing due to the maturity of the process. However, random defects can still occur due to various reasons like the presence of impurities, local wafer defects and human errors.

We conducted investigations on these processes to get information about the types of defects that can occur in them. Looking at processed IC chips, along with the

TABLE I
LAYER DEFINITION OF RSFQ PROCESSES

FOUNDRY1		FOUNDRY2	
Name	Layer	Name	Layer
M2	Nb	R3	Ti/Pd/Au
I2	SiO_2	M3	Nb
R1	Mo	I2	SiO_2
I1B	SiO_2	M2	Nb
I1A	Nb_2O_5	I1B	SiO_2
T1	Nb/ Al_2O_3/ Nb	R2	Mo
M1	Nb	I1A	Nb/ Al_2O_3/ Nb
I0B	SiO_2	M1	Nb
I0A	Nb_2O_5	I0	SiO_2
M0	Nb	M0	Nb

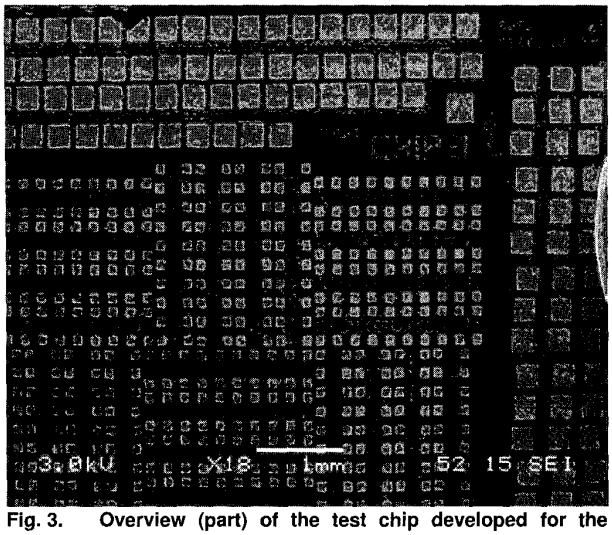

Fig. 3. Overview (part) of the test chip developed for the FOUNDRY1 process; location of the room temperature structures are in the centre and low temperature structures at the periphery for easy access for testing.

design rules, 27 possible defects have been theoretically predicted for the FOUNDRY1 process and 31 for the FOUNDRY2 process. These numbers do not reflect any information about the quality of the process, but are predicted according to the topography of the process. These defects have been grouped and ranked into a list of probable defect locations [14]. The primary defects are related to the thin dielectric-barrier of a JJ. Shorts, opens and pinholes are believed to cause junctions to malfunction. Opens and near opens in metal layers form another high-ranking defect, resulting from the step coverage profile of the underlying SiO_2 isolation layer. Via contact defects due to isolation problems and resistor layer problems are other highly probable defects. Different other possibilities of opens or shorts in the different layers follow.

This initial fault list was used to prepare the test chips by considering the following facts: the frequency of occurrence of the weak-spots and the preferred topography of the defects. They are classified into four groups as shown in Table II. Different structures have been designed and included in the chips to detect them. A brief description of the chips and measurement strategies will be given in the following section.

4. Defect Detection in RSFQ Processes

Test chips have been designed for both foundry processes that allow detection and localization of the predicted defects. Development of simple and easily testable structures was crucial during the design phase. We came up with basically two types of structures. One set for Low Temperature (LT), 4 K measurements and the other set for Room Temperature (RT), 294 K measurements [15]. This reduces unnecessary complexity in the testing phase and test running costs. Fig 3 shows part of the designed test chip for the FOUNDRY1 process.

TABLE II
CLASSIFICATION OF DEFECTS IN LTS RSFQ PROCESSES

Group	Defect Type	Nature of the Defect
1	Junction defects	Shorts, opens or excessive size and number of pin holes in the thin dielectric barrier
2	Metal layer defects	Opens or near opens due to thinning, bridges or shorts due to excessive material
3	Resistor layer defects	Opens or near opens in the metal-to-resistor contact, opens and near opens in the thin Mo resistor layer, bridges or shorts between resistor terminals
4	Isolation layer defects	Opens or near opens resulting in bridges, contact hole problems in via hole

If necessary, the LT structures can be tested at RT and vice versa. This provides a comparison of faulty behaviour at both temperatures. Moreover, study of the faulty behaviour at RT is important because, if those faults at LT can be translated into that at RT, a tremendous gain in test complexity and time and hence costs can be achieved by this approach. The 4 K structures are placed at the four edges of the chip for easy bonding access. The disadvantage of this method is that bonding has to be carried out for the JJ access pads to the circuit board for measurements for each (time-consuming) thermal cycle. The RT structures are positioned at the centre of the chip, which can be accessed by the pins of an automatic prober machine connected to ATE.

4.1 Test Structures

The facts that FOUNDRY1 is a process being developed and FOUNDRY2 is a matured commercial process were used for educated guesses while designing the test chips. Previous studies on the process helped at this stage. Test structures were designed for the various defects listed in Table II. More details on the test structures are given in reference [16].

Fig. 4 shows the photomicrograph of a part of the structure that has been designed for detecting defects in JJs. The measurements are carried out at 4.2 K, analysing the switching properties of a JJ [17]. A method has been developed for detecting and pinpointing possible junction defects. This method has been developed to reduce the number of thermal cycles required, thus reducing test cost and test time [15]. The method consists of an IV-curve

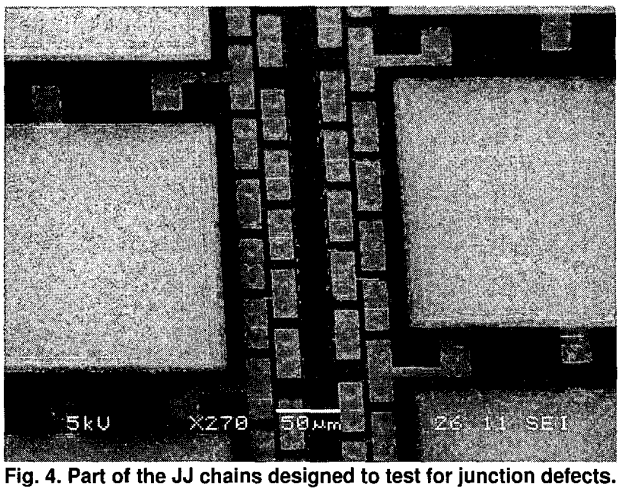

Fig. 4. Part of the JJ chains designed to test for junction defects.

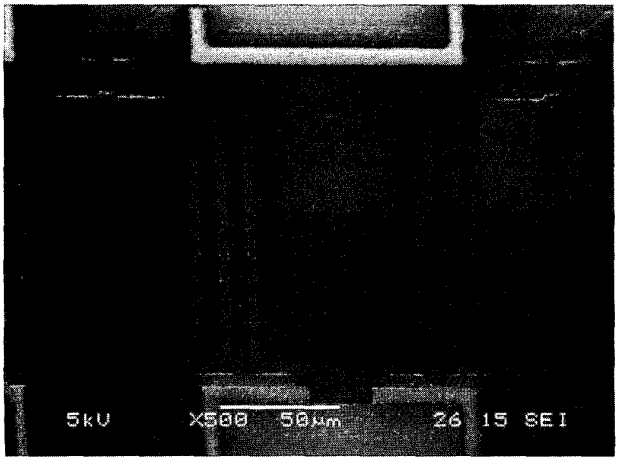

Fig. 5. Part of the structure for the detection of defects in the M2 layer resulting from a step-coverage problem over a via in the FOUNDRY1 process.

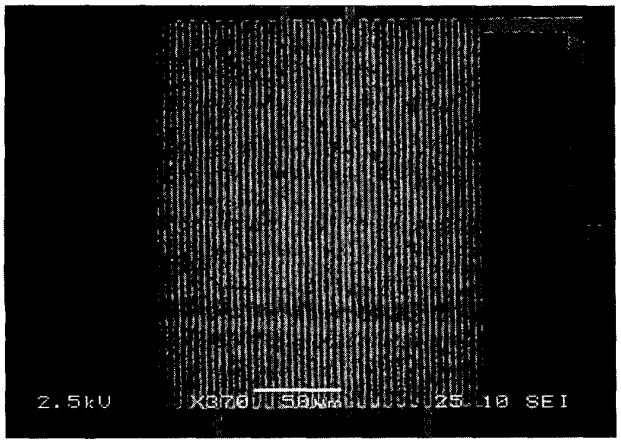

Fig. 6. Part of the structure designed for detection of M2 interconnects problems in FOUNDRY2 process.

measurement on several long series of JJs. The longest chain of 2560 JJs is first evaluated and if a defect is found, further localization is accomplished using the intermediate taps finally trapping the defect down to a segment of 20 JJ in series.

The number of measurements that can be carried out per cycle is also limited depending on the number of the signal lines in the used cryo-probe. With an alternative LT access technique like fingerboard design for the JJ structures, the number of structures that could be placed per chip with reasonable localization of the defect is restricted. Another set of test structures has been designed in which deliberate defects (opens and shorts) have been introduced into the JJs by means of layout modifications. The purpose of this structure is to compare measurements between good and defective JJs, to compare measurement and theory and to develop a realistic fault model for the JJ.

As suggested in [18], step-coverage defects in metal layers can be detected using a structure in which the metal runs over repeated steps of the underlying layer. In SCE, Nb wiring layers running over repeated steps in underlying wiring layers can be used to detect defects at RT. At RT, the resistance of this path is measured and compared with the resistance of a reference path, called "v/d Pol structure" [19], without the steps in the underlying layer. Deviations from the average measured resistance ratio will reveal opens or near opens in any of the test structures.

A structure similar to this has been designed to test for defects in vias. To prevent detecting of multiple defects in the structure, a via step was emulated by removing the corresponding isolation layers and the second metal layer. An example of the design implemented in the FOUNDRY1 process is given in Fig. 5. The structure that has been designed for the detection of shorts in metal layer for the FOUNDRY2 process is shown in Fig. 6.

A similar approach was applied while designing other structures. Table III shows the list of structures that have been developed. The difference in the number of structures is due to the fact that FOUNDRY1 uses very large dimensions (twice the size) as compared to FOUNDRY2 and more basic tests have to be carried out. The second column denotes the number of JJ structures

TABLE III.
LIST OF TEST STRUCTURES DEVELOPED FOR LTS RSFQ PROCESSES

Structure / Process	JJ	Open	Short	Iso	R	Min. Size
FOUNDRY1	9	3	1	4	3	3
FOUNDRY2	2	30	16	18	3	9

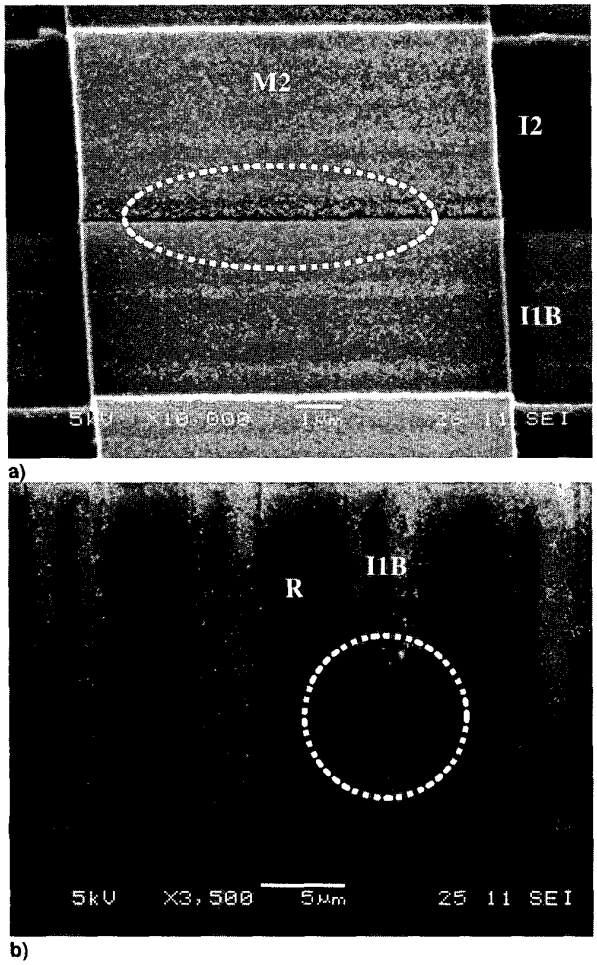

Fig. 7. SEM photographs of detected defects; a) M2 cracking in FOUNDRY1 process and b) bridge in R2 layer in FOUNDRY2 process.

developed. The next two columns are for the metal-layer defects, followed by isolation-layer defects. The sixth column is for the resistor layer structures and the final one for minimum feature-size verification.

4.2 Defect Detection

The basis for the measurements is forcing a current and measuring the voltage at fixed power dissipation. A semi-automatic probe station is used for this purpose. A four-point scheme is being used so that more accurate measurements can be carried out. The measurement data is subjected to analysis, resulting in a list of locations in the structures that are defective. The subsequent locations in the chip are further optically analysed by SEM to confirm the defect.

There are some drawbacks associated with the structures that are process related. For example, the structure that has been designed for resistor-layer defects can only detect complete opens, near opens or complete bridges or shorts in the chain due to the relatively large natural parametric variation of the resistor layer inherent in the process. This could be avoided by taking measurements at all the taps in the structure, which in-turn increases the test time.

Analyses were performed on the processed test chips from both foundries. A number of defects were detected by the designed test structures proving the adopted methodology for the detection of defects. Examples of defects from both processes are given in Fig. 7. Fig. 7a shows the cracking of wiring layer M2 in the FOUNDRY1 process. This is critical as it introduces resistive opens in the circuit. Fig. 7b shows bridging of R2 layer in the FOUNDRY2 process. This layer is used for creating resistance for both biasing and shunting of a JJ. A defect in this layer usually makes the circuit faulty.

The (limited) defect statistics obtained from the above test structures are being used for IFA. Depending upon the type of defect occurring in the processed circuit, it can be classified as semiconductor-like defects and special defects that only apply to superconductor circuits. Resistive bridges and shorts are examples of semiconductor-like defects that can occur in the circuit. Shorts in a JJ are an example of the second kind. The induced faults in the developed test structures will be used to validate the results of our earlier studies [20]. A DOT methodology for RSFQ circuits is discussed in the following section.

5. Defect-Oriented Testing of RSFQ Circuits

In SCE, the present methodology to achieve robust design is by carrying out margin calculations on circuits taking into account the parametric spread and fabricating them with optimum values. To a certain extend, this ensures that the allowed gross process variations and the allowed random local variations will not affect the accepted performance of the circuit. During the test phase, the common practice for digital circuits is to load the data into a shift-register (SR) at low-speed. Subsequently run the system "at-speed" and store the processed data in the output SR. Finally, the read-out is accomplished at a low-speed and the response is subsequently verified. This (functional) test will show whether or not the processed circuit will work. Further information about faults/ defects that might occur is not available from this approach. A DOT approach overcomes this problem because the faults are mapped to the physical defects in the process.

To illustrate the DOT approach, we will be considering a D-type Flip-Flop (DFF). The RSFQ circuit schematic of the DFF is shown in Fig. 8. It consists of 4 JJs (J1 to J4), denoted by "X", 3 inductors (L1 to L3)– 2 normal and a storage inductor, and a bias source (Ib). A bias current of 0.16 mA is sufficient for the operation of this RSFQ DFF. L2 is the storage inductor with J2-L2-J3 forming the super-conducting loop where the data will be stored as a fluxon. Inductances are implemented with the metal wiring layer. In the actual implementation, there will be buffers made of Josephson transmission lines before the inputs and after the outputs, which are not shown in Fig. 8 for the sake of simplicity.

To study the influence of the defects, we applied the DOT strategy to this DFF, which has a maximum operating frequency of 17 GHz at 4.2 K. Both current and logic-based testing approaches were carried out for a better understanding of the test methodology that should be used in SCE circuits. The details of the experiments are given in the following sections.

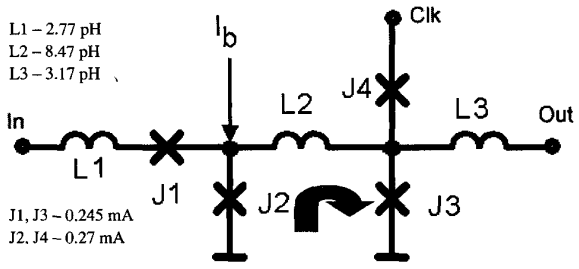

Fig. 8. Circuit scheme of an RSFQ D Flip-Flop.

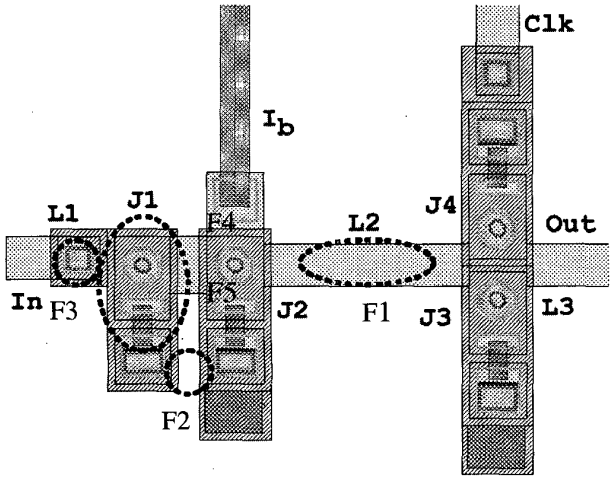

Fig. 9. Layout of an RSFQ D Flip-Flop.

5.1 I_{DDX} Testing

Current testing is an effective methodology in full CMOS semiconductor circuits to analyse structural defects. I_{DDX} testing has not yet been carried out on SCE circuits. An I-V measurement is used to characterize a JJ as mentioned in one of the previous sections. As a JJ is a current-controlled device, a current-based testing technique seems attractive. Eleven faults in the DFF were tested using the I_{DDT} technique. The current flowing through output inductor L3 was monitored during the tests. This can be implemented by inductively coupling L3 with another inductor connected to an SCE amplifier. Different open and shorts were introduced into the circuit for the experiments.

The induced faults were resistive in nature. The information gathered from our earlier study on the faulty behavior of RSFQ circuits [16, 20] was used in the experiments. We found that an introduction of 0.6 Ω was enough for the complete malfunctioning of the circuit. We also observed that the circuits start misbehaving, even when the value of the induced resistor is as low as 60 mΩ. This is due to the fact that RSFQ circuits woks in the super-conducting state. For the experiments described in this paper, each time we introduced the minimum resistance that was able to produce a detectable faulty behavior in the circuit and the corresponding currents were measured.

An example of a simple layout of an RSFQ DFF is given in Fig. 9. The locations of the introduced faults are marked. The first fault to be introduced was the crack in the storage inductor L2, denoted by "F1". Here a 0.5 Ω resistor was introduced. The next fault (F2) that was considered is the short in the node connecting J1 and J2 to ground. This is possible if a short is present between the M1 layers of the grounded and the un-grounded junction, connecting the above-mentioned node to ground. In this case a 0.43 Ω resistor was introduced in the netlist. The third fault (F3) that has been introduced is resulting from the M1-M2 via problem and a 0.6 Ω resistor was introduced in this case. The next 8 faults (F4-F11: only shown on J1, F4 and F5, for simplicity) were the shorts and opens in the thin barrier of the 4 JJs present in the circuit. In the case of a short, a 0.1 Ω resistor was introduced in parallel to the JJ and a 100 Ω resistor was introduced in the Spice model of the JJ for the open case.

The experiments were carried out using JSIM (Josephson Simulator) – a Spice variant for RSFQ circuits. The experimental data was analysed using MATLAB. One of the plot results is given in Fig. 10. The defect is a crack in the storage inductor L2. It shows that the defect is detectable using this technique. Note that the currents are

small in magnitude, but compared to the current in a defect-free circuit, about 50% change in value was observed. Those experiments resulting in less than 25% deviations were considered to be undetectable. While performing the tests, the normal input was replaced by a constant voltage source.

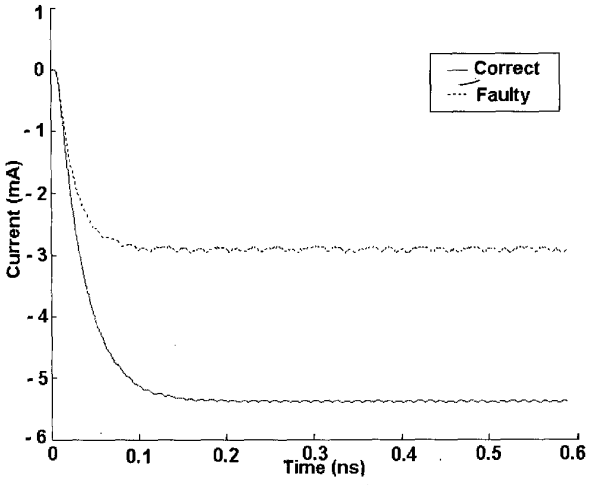

Fig. 10. Defect detection in a DFF using I_{DDT} testing.

5.2 Logic-based Structural Testing

As mentioned before, a functional test is commonly used in SCE for verification of the design implementation. We used the same 11 faults as before in a logic-based structural test for comparison with current testing. Similar approaches as in [16, 20] were used for analysis. The following malfunctions were observed while testing:

a) The input signals were influenced by the defect and resulted in incorrect operation.

b) The output signals were delayed for a certain period depending on the severity of the fault.

c) No response resulted from the output ports.

In other cases, the input or output signals were slightly distorted, but the logic operations were not affected making such defects undetectable using logic-based testing. Fig 11 shows the test results. Fig 11a shows the defect-free operation of a DFF. In all cases, the same test vectors were used. Fig 11b shows the case A as explained above and case C is seen in Fig 11c. Case A was observed when the second fault (F2) as mentioned in the previous sub-section was introduced, i.e. the JJ nodes connecting J1 and J2 shorted to ground. Case b was observed when the assumed fault was crack in L2 (F1). On introducing the M1-M2 via fault (F3), case B was observed. These are

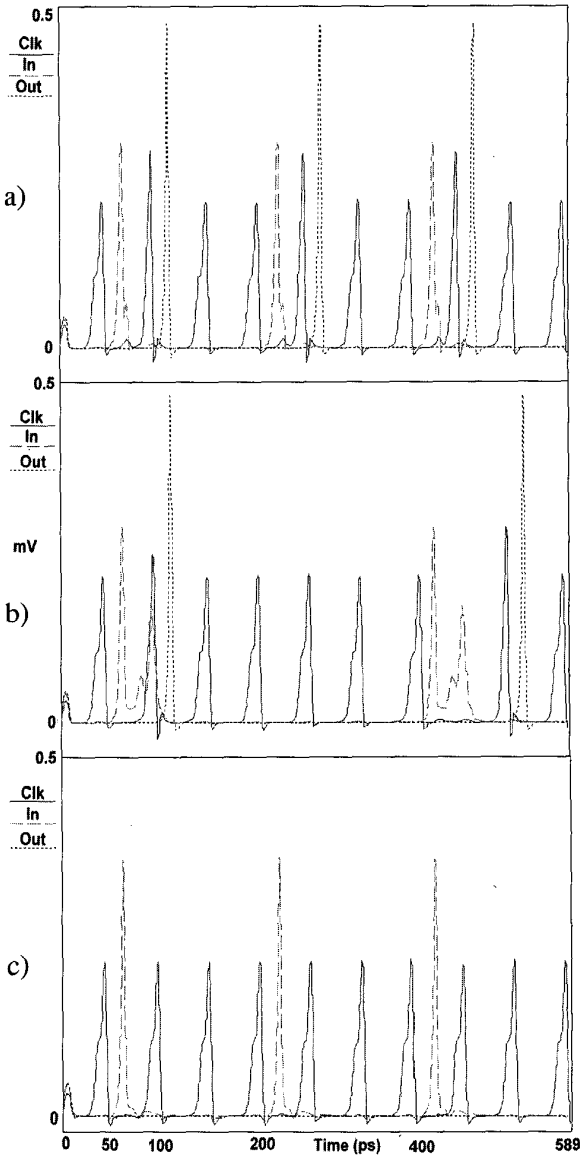

Fig. 11. Defect detection using logic-based testing: Fault-free case (a) and faulty DFF testing results (b, c).

SFQ pulses of very small magnitude (up to a few mV). They have to be amplified using SCE amplifiers before applying them to conventional test equipment.

6. Experimental Results

The results of the experiments are given in Table IV. The second column provides the details of the faults induced. These opens and shorts were introduced in JJs, interconnects and vias. The reason for some of the defects in one branch (for e.g. input) of the circuit that affects the

functionality of others (e.g. clock), is that SCE circuits operate in a super-conducting state. A defect in one of the elements in the super-conducting loop influences the other element and is in many cases indistinguishable.

From the results, shorts or bridges are easy to detect while opens tends to escape the test. All the introduced bridging-faults could be detected by logic-based testing. This could again be due to the super- conducting loops. From the results until now, we may assume that I_{DDT} testing does not provide more information in the case of SCE circuits, contrary to that in the case of silicon semiconductor circuits. A more detailed study has to be carried out to verify these arguments. These results will then be used for a more realistic study of DOT at system-level like complete ADCs and microprocessors for SCE as mentioned in reference [21].

7. Conclusions

In this paper, the defect-oriented methodology has been discussed for the development of structural testing of complex SCE. This is the start towards a systematic DOT scheme for RSFQ circuits. We presented case studies of two superconductor foundries: an academic and a commercial foundry. Classification of structural defects has been carried out for LTS RSFQ processes. We have developed test chips for the detection of the defects for statistical studies for IFA analysis. Tests carried out on the processed structures proved that the approach is capable of detection of defects in the process.

The information gained from the above study is then used for DOT of complex RSFQ digital circuits. We have carried out Iddx testing for the first time in SCE. A comparison of the test results was carried out with respect to logic-based structural testing. At this stage, we were not able to find any additional benefits with current testing as in semiconductors; in fact less defects were detected using current testing. But a more detailed study is required before making general conclusions.

Due to the above reasons, we are not yet able to draw a final conclusion on whether or not conventional ATPG techniques used in semiconductors is fully applicable to SCE. A significant portion of research is still ahead with respect to verification of fault models and ATPG for SCE.

TABLE IV.
TESTING OF AN RSFQ DFF

DFF Testing	Induced Faults		Detectable		Undetected	
	Open	Short	Open	Short	Open	Short
Current testing	6	5	2	3	4	2
Logic testing	6	5	4	5	2	0

8. Acknowledgements

This research is being carried out within the "TeraHertz" strategic orientation of the MESA+ Research Institute. The authors are indebted to the members of both foundries for their assistance in preparing the required data and chip design. We would also like to thank Mr. Bert Otter of MESA+ Clean room for providing assistance in SEM analysis.

9. References

[1] J. Mitola, "Software radio architecture evolution: foundations technology tradeoffs, and architecture implications", IEICE Trans. Commun. E83-B (2000) pp. 1165–1173.

[2] Y. Oyanagi, "Future of supercomputing", J. Comp. Appl. Math., Vol. 149/1, Dec 2002, pp. 147-153

[3] B. Sultan "A switch-router taxonomy", Comp. Commun., Vol. 21/2, March 1998, pp. 101-110

[4] K. Saitoh et al., "Evaluation of Dynamic Range for an HTS Sigma-Delta Modulator with 100-GHz Sampling", 2EM03, Proc. IEEE Applied Superconductivity Conference 2002, Houston, USA, Aug 2002.

[5] K. Likharev, Rapid single flux quantum (RSFQ) logic, Encyclopaedia of Materials, Science and Technology, Elsevier, 2002, an electronic version of the document is available at: http://www.elsevier.com/mrwclus/15/183/35/index.htt.

[6] L. Yu et al., "An all-niobium eight level process for small and medium scale applications", IEEE Trans. Magnet., Vol. 23/2, Mar 1987 pp. 1476 –1479.

[7] O. A. Mukhanov et al., "High Resolution ADC Operation up to 19.6 GHz Clock Frequency", Supercond. Sci. Technol., Vol. 14, Nov 2001, pp. 1065-1070.

[8] M Dorojevets et al., "Flux Chip: Design of a 20-GHz 16-bit Ultra pipelined RSFQ Processor Prototype Based on 1.75-mm LTS Technology", IEEE Trans. Appl. Supercond., Vol. 11/1, Mar 2001, pp. 326-332.

[9] S. Yorozu et al., "Single Flux Quantum Packet Switch Circuits for Large-scale Communication Systems", 1EM08, Proc. IEEE Applied Superconductivity Conference 2002, Houston, USA, Aug 2002.

[10] J. Pineda de Gyvez and D.K. Pradhan "Integrated Circuit Manufacturability – The Art of Process and Design Integration", IEEE Press, New York 1999, ISBN 0-7803-3447-7.

[11] S. Sengupta et. al. "Defect-Based Test: A Key Enabler for Successful Migration to Structural Test" Intel Technology Journal Q1'99, e-copy can be obtained from web address http://developer.intel.com/technology/itj/q11999/articles/art_6.htm

[12] K. K. Likharev, "Dynamics of Josephson Junctions and Circuits", Gordon and Breach, New York, 1986.

[13] K. Gaj et al., "Toward a systematic design methodology for large multigigahertz rapid single flux quantum circuits", IEEE Trans. Appl. Supercond., Vol. 9/3, Sep 1999, pp. 4591 -4606

[14] A.A. Joseph et al., "The Detection of Defects in a Niobium Tri-layer Process", IEEE Trans. Appl. Supercond., Vol. 13/2, Jun 2003, scheduled to be published. (Copy available from the author).

[15] S. Heuvelmans, "A Test methodology for analyzing defects in LTS RFSQ circuits", M.Sc. thesis, University of Twente, The Netherlands, July 2002.

[16] A.A. Joseph et al., "Test Structures and their Application in Structural Testing of Digital RSFQ Circuits", PHYSICA C 2003, to be published. (A copy of the paper can be obtained from the author).

[17] R. Monaco, et al., "Fabrication and properties of multiple vertically stacked Josephson tunnel junctions", IEEE Trans. Appl. Supercond., Vol. 6/1, Mar 1996, pp. 32-37.

[18] A. Jakubowski, et al., "Diagnostic measurements in LSI/VLSI integrated circuits production", World Scientific publishing Co., 1991, ISBN 981-0202-82-2.

[19] J.A. van der Pol, " Short Loop Monitoring of Metal Step Coverage by Simple Electrical Measurements", in Proc. IEEE IRPS, 1996, pp. 148-155.

[20] H. G. Kerkhoff and H. Speek, "Defect-Oriented Testing of Josephson Logic Circuits and Systems", Physica C, vol. 350, Feb. 2001, pp. 261-268.

[21] A. A. Joseph, M.H.H. Weusthof and H. G. Kerkhoff, "Application of DfT techniques to a 20 GHz superconductor delta ADC", Micro. Elec. Jour. Vol. 33/10, Oct. 2002, pp. 791-798.